

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Shreesh Narasimha, et al.	Examiner:	Unassigned
Serial No.:	Unassigned	Art Unit:	Unassigned
Filed:	Herewith	Docket:	FIS920020200US2(16106A)
For:	CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE	Date:	January 23, 2004

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

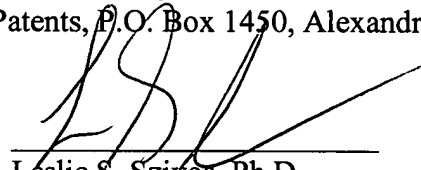
In connection with filing the above-identified application under 37 C.F.R.
§1.53(b), applicants submit the following amendments and remarks for consideration by the
Examiner and entry of record in the above-identified patent application.

CERTIFICATE OF MAILING BY EXPRESS MAIL

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Date of Deposit:	January 23, 2004

I hereby certify that this correspondence is being deposited with the United States Postal Service Express Mail Post Office to Addressee service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 23, 2004.

Dated: January 23, 2004


Leslie S. Szivos, Ph.D.